HT32 Peripherals

32位元產品應用開發處
CG10

HT32F5 Series
(M0+)

Feature List – 52342/52

Peripherals		HT32F52342	HT32F52352
Main Flash (KB)		64	127.5
Option Bytes Flash (KB)		0.5	0.5
SRAM (KB)		8	16
Timers	MCTM	1	
	GPTM	2	
	SCTM	2	
	BFTM	2	
	RTC	1	
	WDT	1	
Communication	USB	1	
	SPI	2	
	USART	2	
	UART	2	
	I²C	2	
	I²S	1	
	SCI (ISO7816-3)	2	
EBI		1	
CRC-16/32		1	
GPIO		Up to 51	
EXTI		16	
12-bit ADC		1	
Number of channels		12 Channels	
Comparator		2	
CPU frequency		Up to 48 MHz	
Operating voltage		2.0 V ~ 3.6 V	
Operating temperature		-40° C ~ +85° C	
Package		48/64-pin LQFP	

Power Saving Mode – 52342/52

Symbol	Mode	Conditions	CP Pass Avg.	Unit
I_{VDD}	Run	f_{HCLK} = 48 MHz, f_{PCLK} = 48 MHz, All peripherals enabled	19.4	mA
		f_{HCLK} = 48 MHz, f_{PCLK} = 48 MHz, All peripherals disabled	9.86	mA
	Sleep	f_{HCLK} = 0 MHz, f_{PCLK} = 48 MHz, All peripherals enabled	12.5	mA
		f_{HCLK} = 0 MHz, f_{PCLK} = 48 MHz, All peripherals disabled	2.58	mA
	Deep-Sleep1	All clock off (HSE/PLL/f_{HCLK}), LSI/RTC on, LDO in low power mode	37.3	uA
	Deep-Sleep2	All clock off (HSE/PLL/f_{HCLK}), LSI/RTC on, LDO off (DMOS on)	9.5	uA
	Power-Down	V_{DD} = VBAT = 3.3 V, LDO off, LSE off, LSI on, RTC on	1.68	uA
		V_{DD} = VBAT = 3.3 V, LDO off, LSE off, LSI on, RTC off	1.63	uA
I_{BAT}	Power-Down	V_{DD} not present, VBAT = 3.3 V, LDO off, LSE off, LSI on, RTC on	1.35	uA
		V_{DD} not present, VBAT = 3.3 V, LDO off, LSE off, LSI on, RTC off	1.34	uA

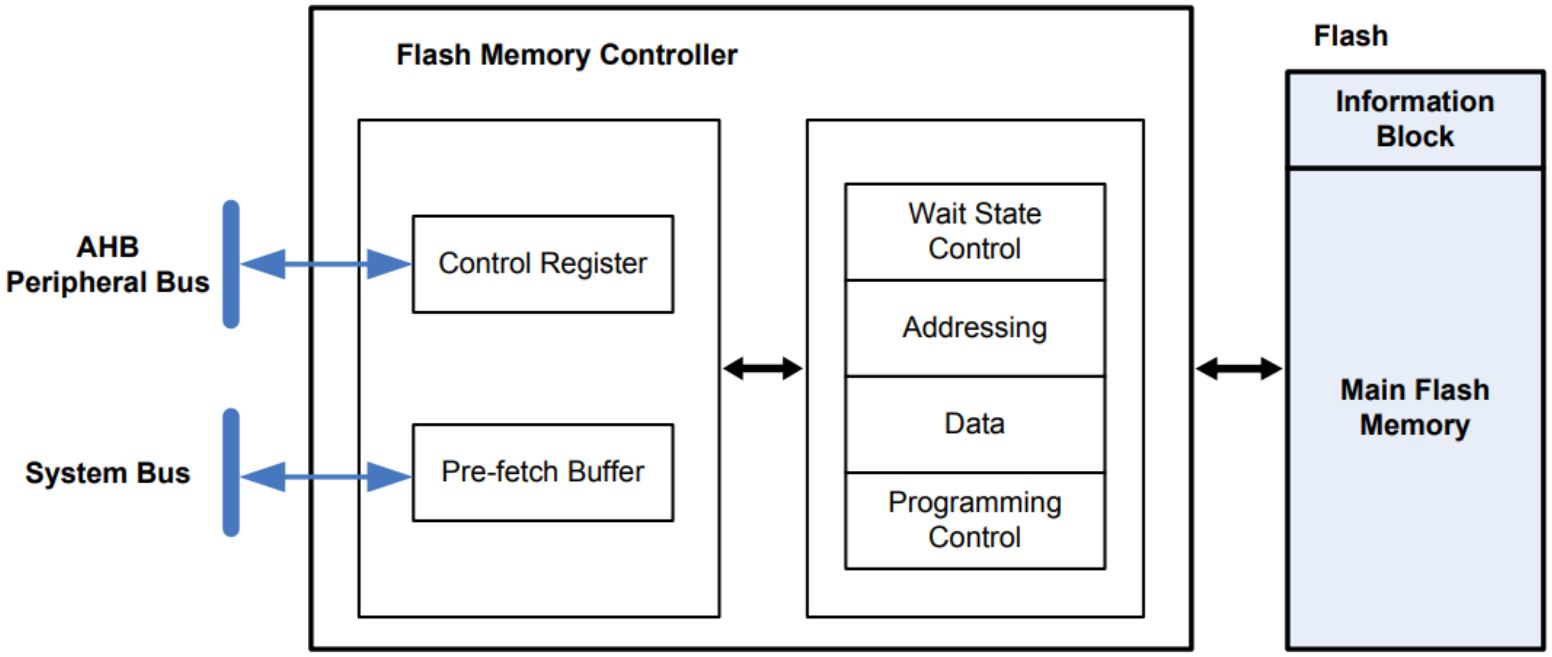
V_{DD} = 3.3 V, HSE = 8 MHz, PLL = 48 MHz

HT32F52342/52 Peripherals

Property	Peripheral Name
System	FMC, PWRCU, CKCU, RSTCU, PDMA
IO	GPIO, AFIO, EXTI
Functional	ADC, I²S, CRC
Timers	BFTM, GPTM, MCTM, RTC, WDT
Communication	I²C, SPI, USART, UART, USB, SCI, EBI

Flash Memory Controller (FMC)

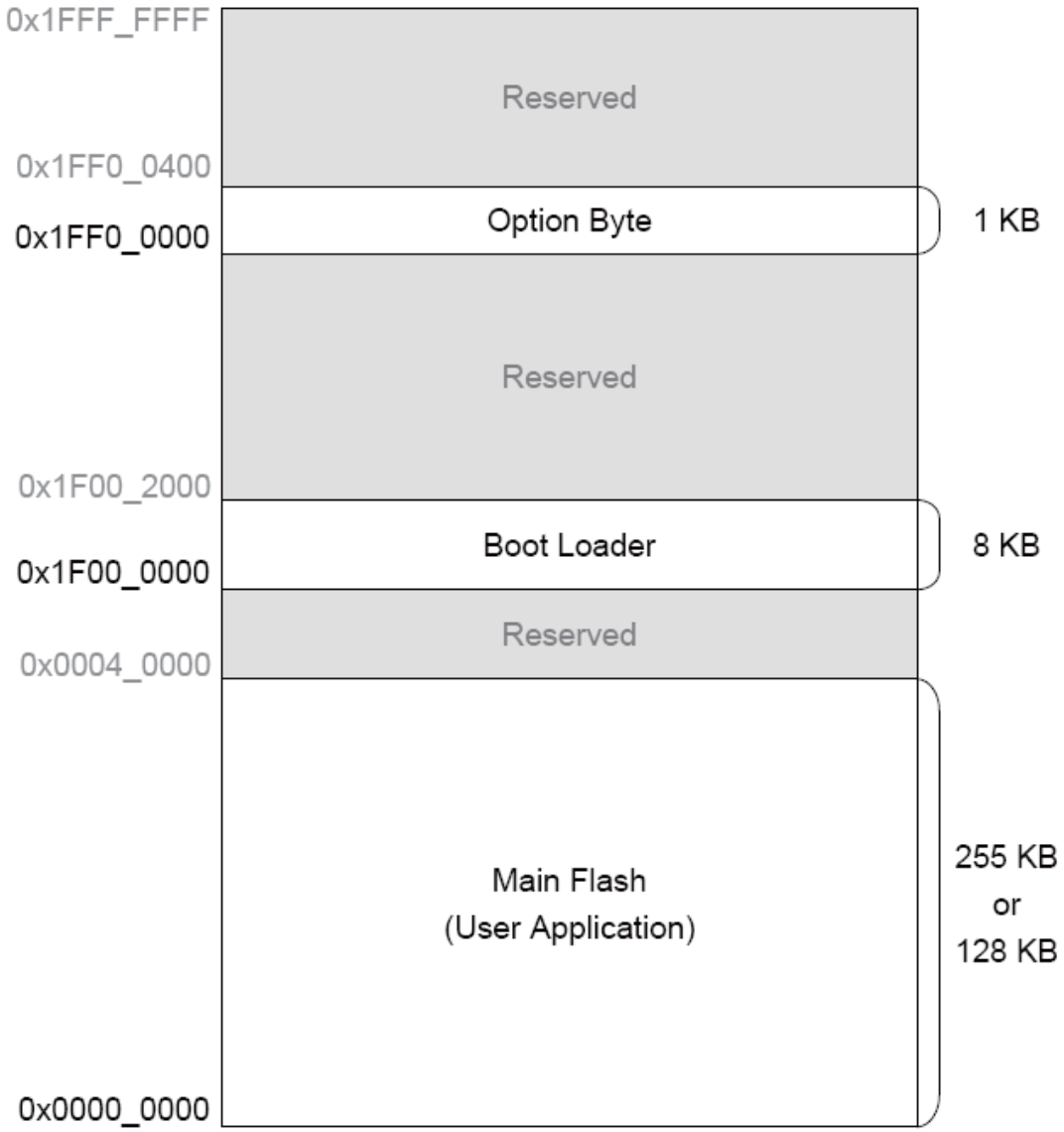
FMC - Block Diagram



FMC - Features

- Up to 128 KB of on-chip Flash memory for storing instruction/data and options
  - 128 KB (instruction/data + Option Byte)
  - 64 KB (instruction/data + Option Byte)
- Page size of 512 Bytes, totally up to 256 pages depending on the main Flash size
- Wide access interface with pre-fetch buffer to reduce instruction gaps
- Page erase and mass erase capability
- 32-bit word programming
- Interrupt capability when ready or error occurs
- Flash read protection to prevent illegal code/data access
- Page erase/program protection to prevent unexpected operation

FMC - Memory Map



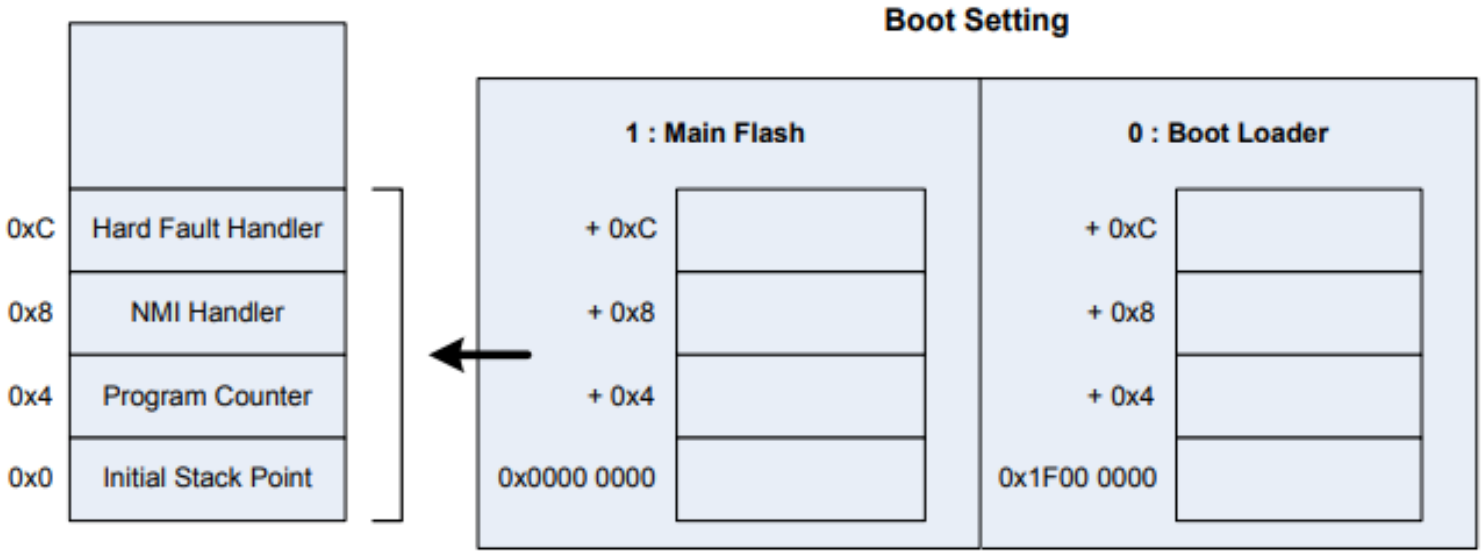
FMC - Memory Architecture

Block	Name	Address	Page Protection Bit	Size
Main Flash Block	Page 0	0x0000_0000 ~ 0x0000_01FF	OB_PP [0]	512 Bytes
	Page 1	0x0000_0200 ~ 0x0000_03FF		512 Bytes
	Page 2	0x0000_0400 ~ 0x0000_05FF	OB_PP [1]	512 Bytes
	Page 3	0x0000_0600 ~ 0x0000_07FF		512 Bytes
	⋮	⋮	⋮	⋮
	Page 252	0x0001_F800 ~ 0x0001_F9FF	OB_PP [126]	512 Bytes
	Page 253	0x0001_FA00 ~ 0x0001_FBFF		512 Bytes
	Page 254	0x0001_FC00 ~ 0x0001_FDFF	OB_PP [127]	512 Bytes
	Page 255 (Option Byte)	Physical: 0x0001_FE00 ~ 0x0001_FFFF Alias: 0x1FF0_0000 ~ 0x1FF0_01FF	OB_CP [1]	512 Bytes
Information Block	Boot Loader	0x1F00_0000 ~ 0x1F00_0FFF	NA	4 KB

Notes: 1. Information Block stores boot loader, this block can not be programmed or erased by user.
2. Option Byte is always located at last page of main Flash block.

FMC - Booting Modes

Booting mode selection pin BOOT	Mode	Descriptions
0	Boot Loader	The source of Vector is Boot Loader
1	Main Flash	The source of Vector is main Flash



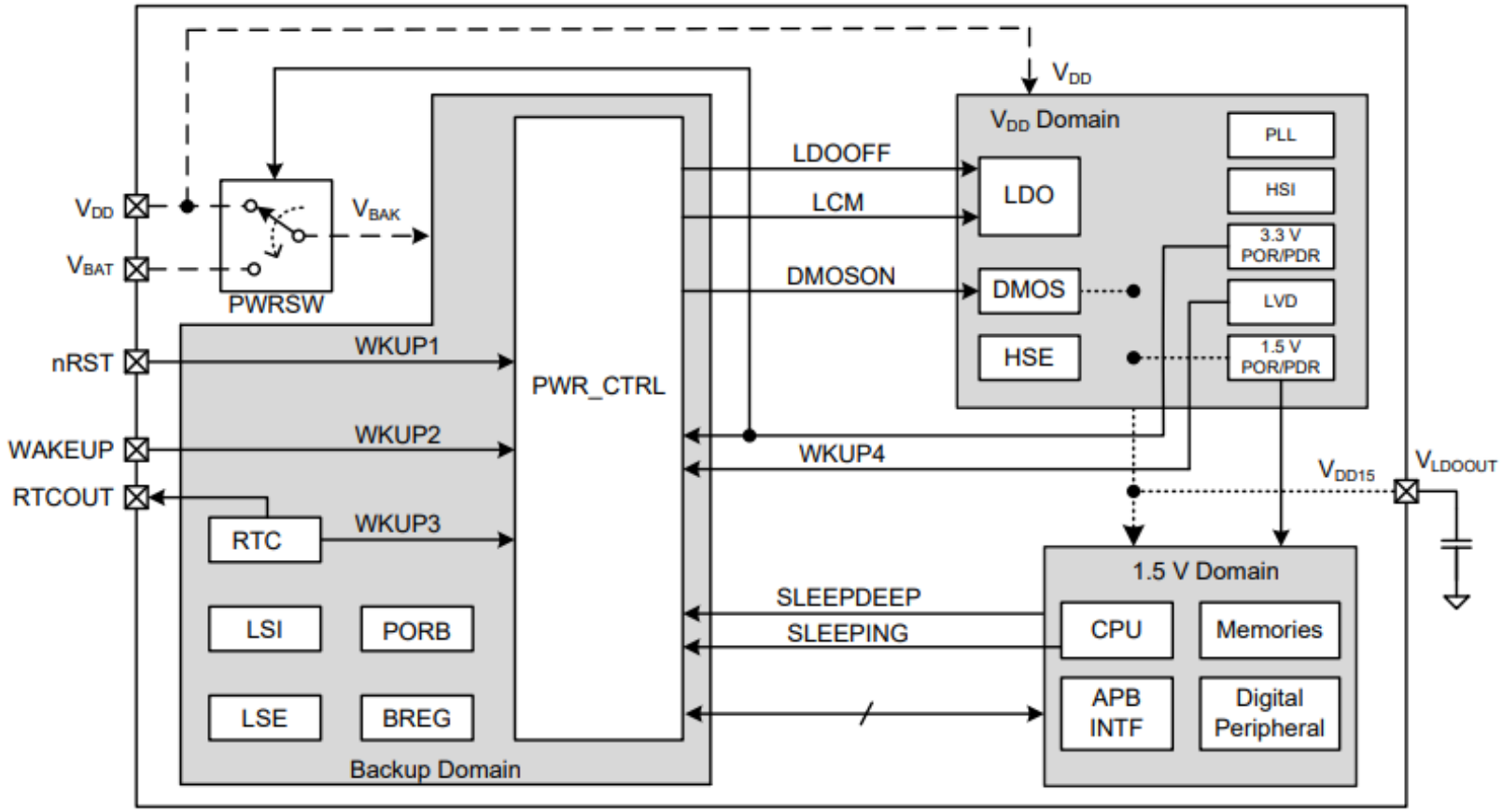
FMC - Wait State

Wait State Cycle	HCLK
0	0 MHz < HCLK <= 24 MHz
1	24 MHz < HCLK <= 48 MHz

- HCLK clock is changed from lower to higher: Change the wait state setting first and then change the HCLK clock.
- HCLK clock is changed from higher to lower: Change the HCLK clock first and then change the wait state setting.

Power Control Unit (PWRCU)

PWRCU - Block Diagram



PORB: V_{BAK} Power On Reset
BREG: Backup Registers

LDO: Voltage Regulator
DMOS: Depletion MOS

LVD: Low Voltage Detector
POR/PDR: Power On Reset/Power Down Reset

PWRCU - Features

- Three power domains: Backup, V_{DD} and 1.5 V power domains.
- Four power saving modes: Sleep, Deep-Sleep1, Deep-Sleep2 and Power-Down modes.
- Internal Voltage regulator supplies 1.5 V voltage source.
- Additional Depletion MOS supplies 1.5 V voltage source with low leakage and low operating current.
- A power reset is generated when one of the following events occurs:
  Power-on / Power-down reset (POR / PDR reset).
  When exiting Power-Down mode.
  The control bits BODEN = 1, BODRIS=0 and the supply power $V_{DD} \leq V_{BOD}$.
- BOD Brown Out Detector can issue a system reset or an interrupt when V_{DD} power source is lower than the Brown Out Detector voltage V_{BOD}.
- LVD Low Voltage Detector can issue an interrupt or wakeup event when V_{DD} is lower than a programmable threshold voltage V_{LVD}.
- Switch Battery power (V_{BAT}) for backup domain when V_{DD} is lower than V_{PDR} voltage.
- 40 bytes of backup registers powered by V_{BAK} for data storage of user application data when in the Power-Down mode.

PWRCU – Operation Modes

Mode name	Hardware Action
Run	After system reset, CPU fetches instructions to execute.
Sleep	1. CPU clock will be stopped. 2. Peripherals, Flash and SRAM clocks can be stopped by setting.
Deep-Sleep1 ~ 2	1. Stop all clocks in the 1.5 V power domain. 2. Disable HSI, HSE, and PLL. 3. Turning on the LDO low current mode or DMOS to reduce the 1.5 V power domain current.
Power-Down	Shut down the 1.5 V power domain

PWRCU - Power Saving Modes

Mode	Mode Entry				Mode Exit
	CPU Instruction	CPU SLEEPDEEP	LDOOFF	DMOSON	
Sleep	WFI or WFE (Takes effect)	0	X	X	WFI: Any interrupt WFE: Any wakeup event (1) or Any interrupt (NVIC on) or Any interrupt with SEVONPEND = 1 (NVIC off)
Deep-Sleep1		1	0	0	Any EXTI in event mode or RTC wakeup or CMP Wakeup or LVD wakeup (2) or WAKEUP pin rising edge or USB resume
Deep-Sleep2		1	X	1	RTC wakeup or LVD wakeup (2) or WAKEUP pin rising edge
Power-Down		1	1	0	RTC wakeup or LVD wakeup (2) or WAKEUP pin rising edge or External reset (nRST)

System Control Register (SCR [2])

Backup Domain Control Register (BAKCR [3])

Backup Domain Control Register (BAKCR [7])

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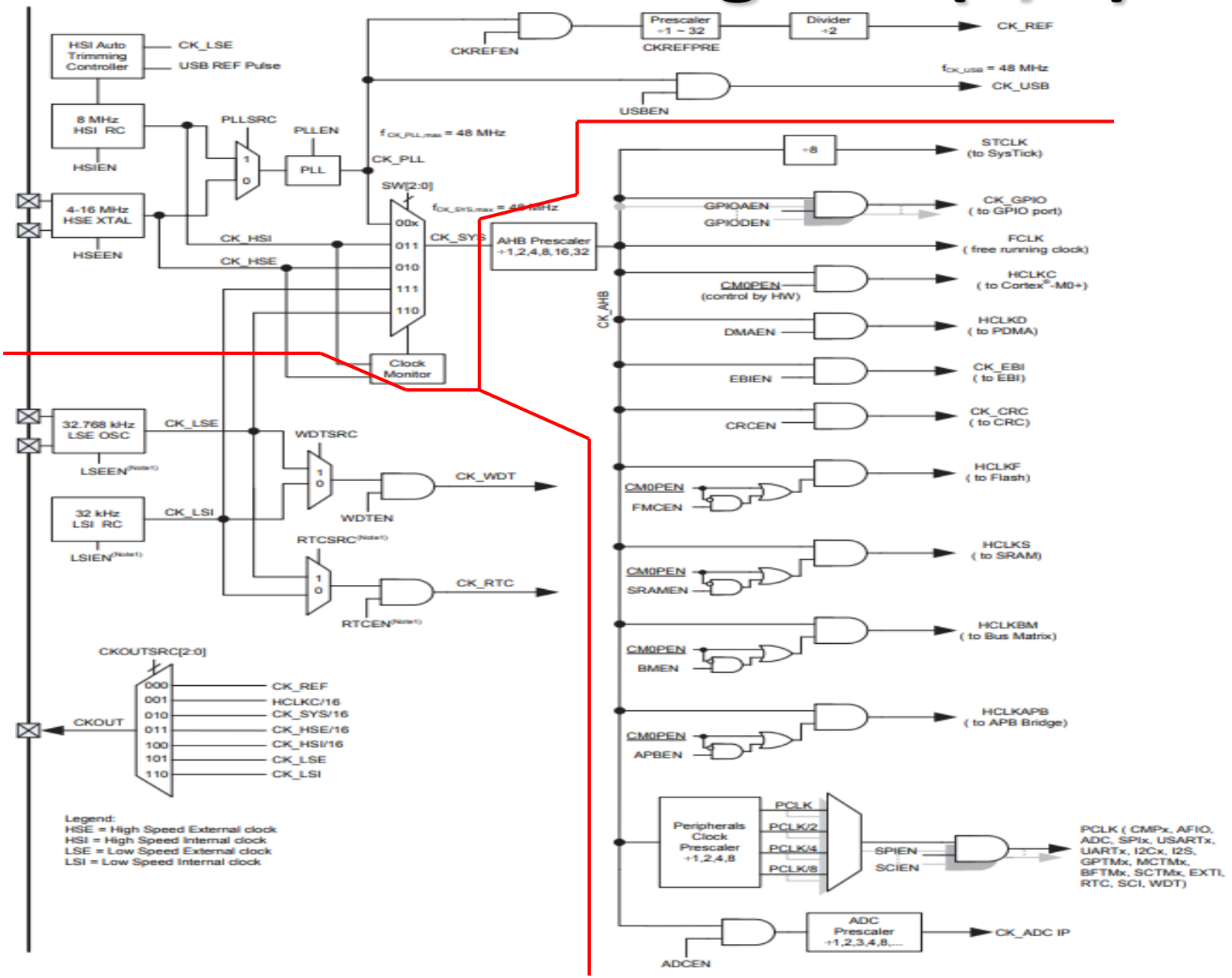
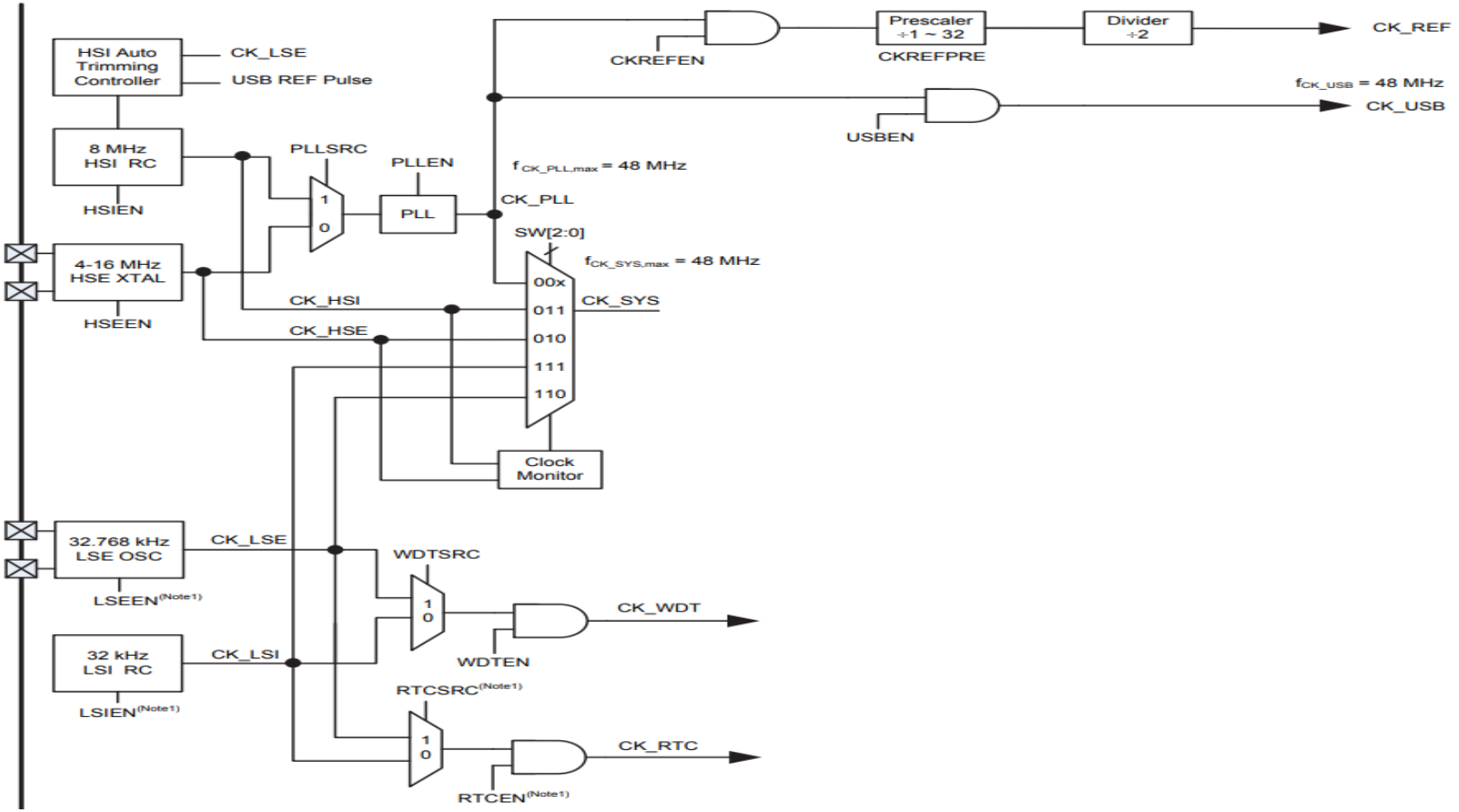
Clock Control Unit (CKCU)

CKCU - Block Diagram (1/4)



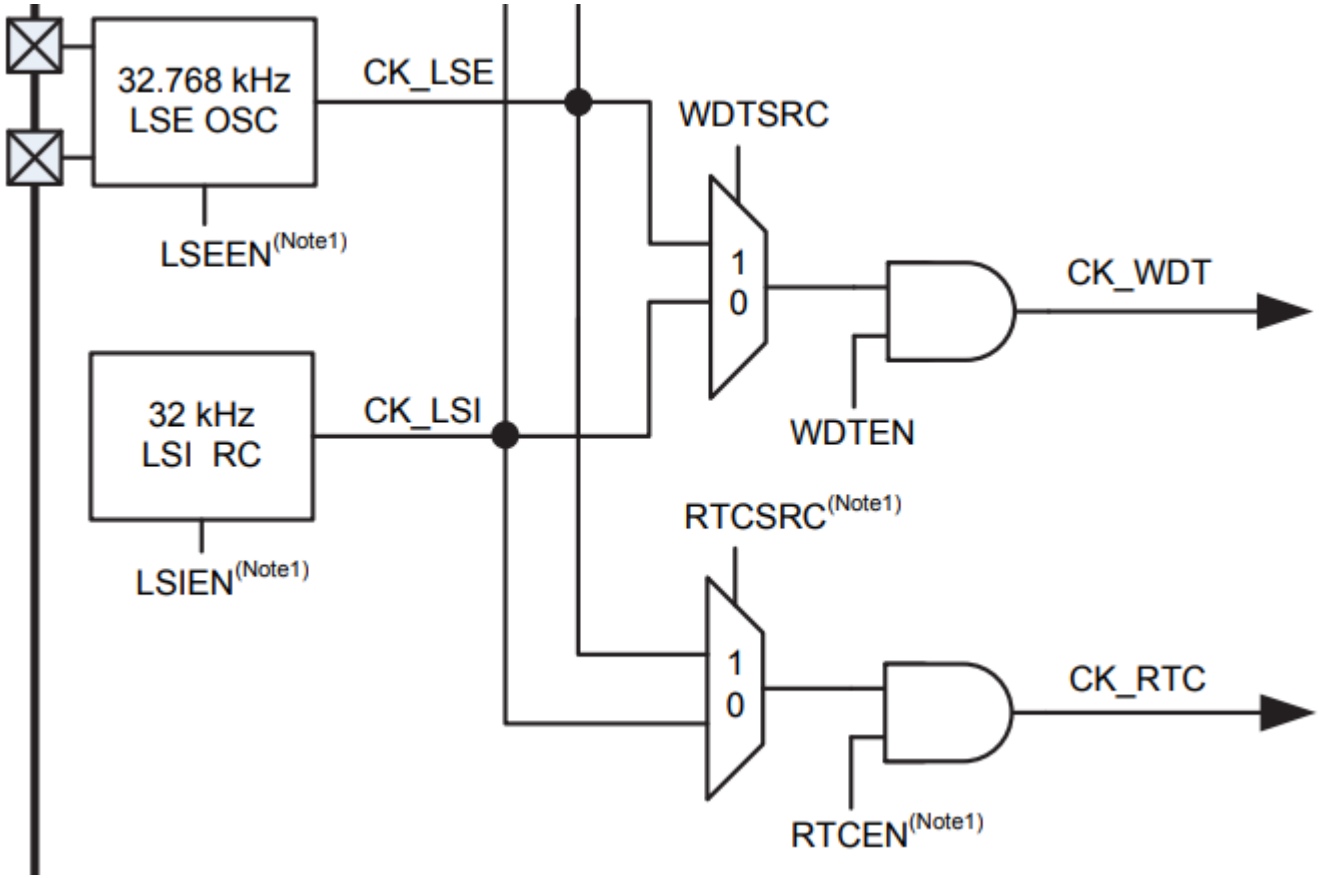
CKCU - Block Diagram (2/4)

- System clock (CK_SYS) sources from HSI, HSE, LSI, LSE or PLL and up to 48 MHz.
- HSE Clock Monitor.

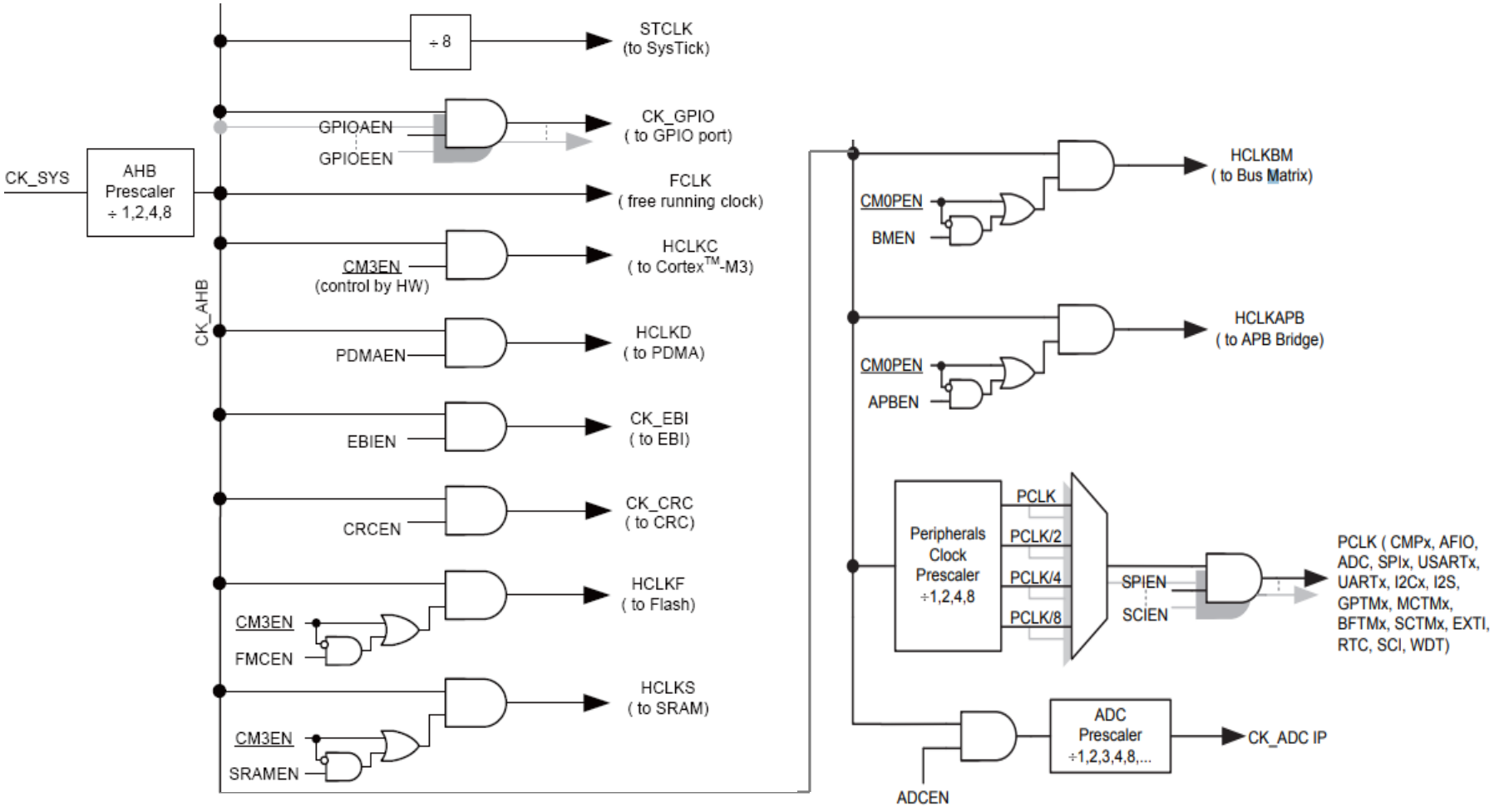


CKCU - Block Diagram (3/4)

- **Watchdog Timer (CK_WDT) and Real Time Clock (CK_RTC) use either LSI or LSE as clock source.**



CKCU - Block Diagram (4/4)



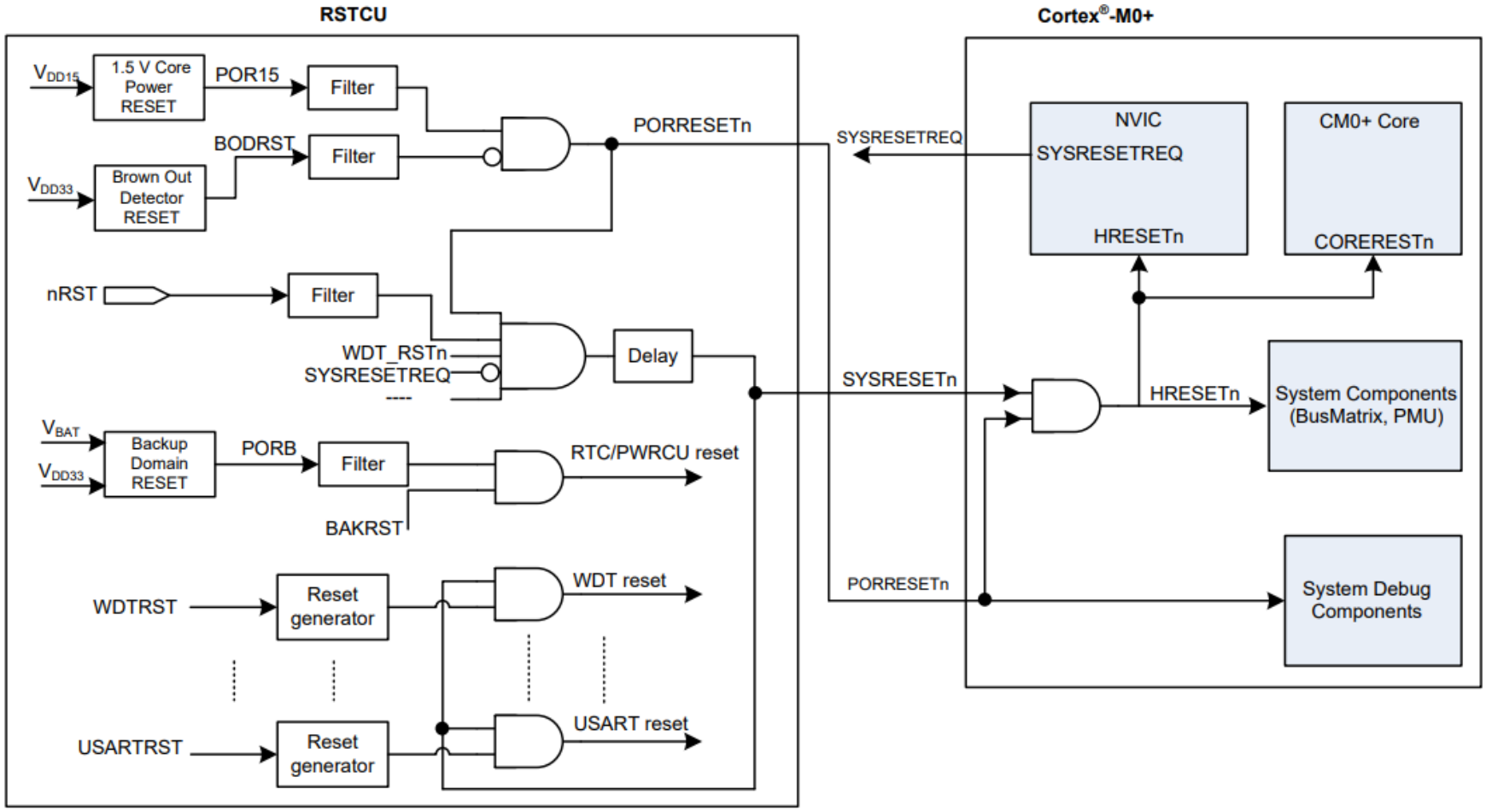
CKCU - Features

- 4 ~ 16 MHz external crystal oscillator (HSE)
- Internal 8 MHz RC oscillator (HSI) with configuration option calibration and custom trimming capability.
- PLL with selectable clock source (from HSE or HSI) for system clock.
- 32,768 Hz external crystal oscillator (LSE) for Watchdog Timer, RTC or system clock.
- Internal 32 kHz RC oscillator (LSI) for Watchdog Timer, RTC or system clock.
- HSE clock monitor

Reset Control Unit (RSTCU)

RSTCU - Block Diagram

- **Three kinds of reset, power on reset, system reset and APB unit reset.**



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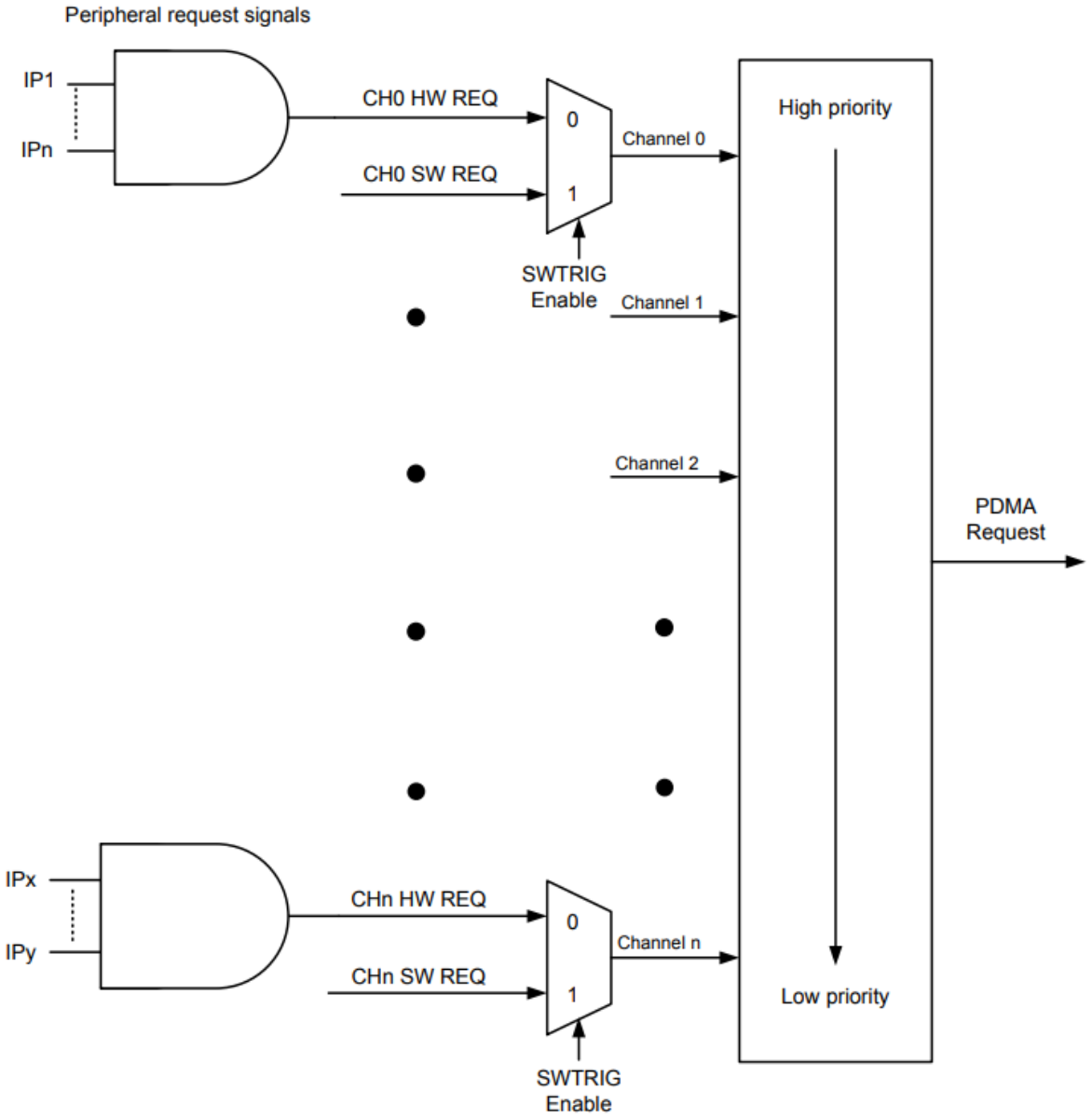
Peripheral Direct Memory Access (PDMA)

PDMA - Features

- 6 unidirectional PDMA channels
- Memory-to-peripheral, peripheral-to-memory and memory-to-memory data transfer
- 8-bit, 16-bit and 32-bit width data transfer
- Software and hardware requested data transfer with configurable channel priority
- Linear, circular and non-increment address modes
- 4 transfer event flags – Transfer complete, Half Transfer, Block End and Transfer Error
- Auto-Reload function

PDMA – Request



PDMA – Channel

IP (x=0,1)	PDMA Channel Number					
	CH0	CH1	CH2	CH3	CH4	CH5
ADC	ADC					
SPIx	SPI0_RX	SPI0_TX			SPI1_RX	SPI1_TX
USARTX	USR0_RX	USR0_TX	USR1_RX	USR1_TX		
UARTX			UR0_RX	UR0_TX	UR1_RX	UR1_TX
SCIx			SCI1_RX	SCI1_TX	SCI0_RX	SCI0_TX
I2Cx			I2C0_RX	I2C1_RX	I2C0_TX	I2C1_TX
MCTM	MT_CH0	MT_TRIG	MT_CH1	MT_CH2	MT_CH3 MT_UEV2	MT_UEV1
GPTMx	GT0_CH1 GT0_CH3	GT0_CH2 GT0_UEV	GT0_CH0 GT0_TRIG	GT1_CH0 GT1_CH3	GT1_CH1 GT1_UEV	GT1_CH2 GT1_TRIG
I^2S		I2S_RX	I2S_TX			

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General Purpose I/O (GPIO)

GPIO - Features

- Input/output direction control
- Schmitt Trigger Input function enable control
- Input weak pull-up/pull-down control
- Output push-pull/open drain enable control
- Output set/reset control
- Output drive current selection
- External interrupt with programmable trigger edge - using EXTI configuration registers
- Analog input/output configurations – using AFIO configuration registers
- Alternate function input/output configurations - using AFIO configuration registers
- Port configuration lock

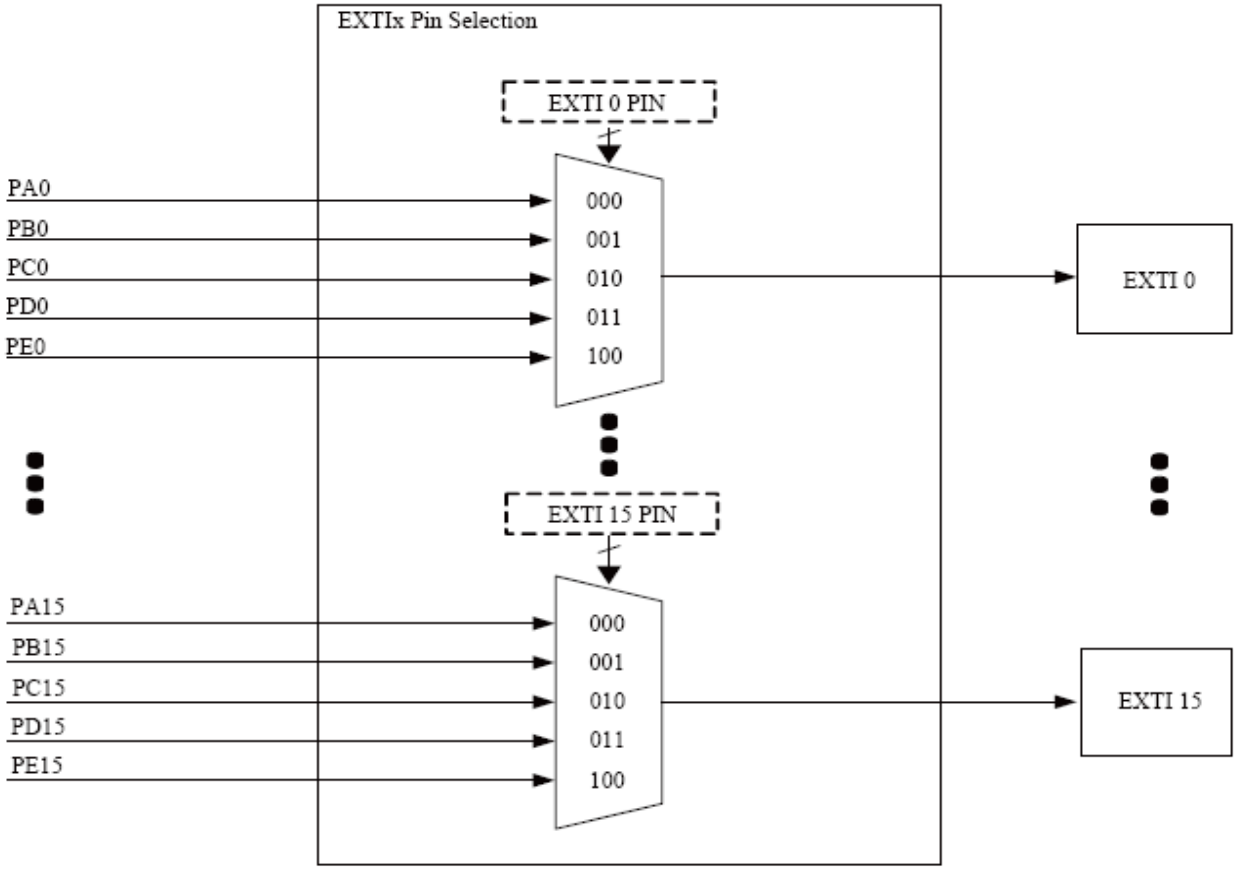
GPIO - Default Pin Configuration

- PA8: Input enable with internal pull-up
- PA9_BOOT: Input enable with internal pull-up
- SWCLK: Input enable with internal pull-up
- SWDIO: Input enable with internal pull-up

Alternate Function I/O Control Unit (AFIO)

AFIO - Features (1/2)

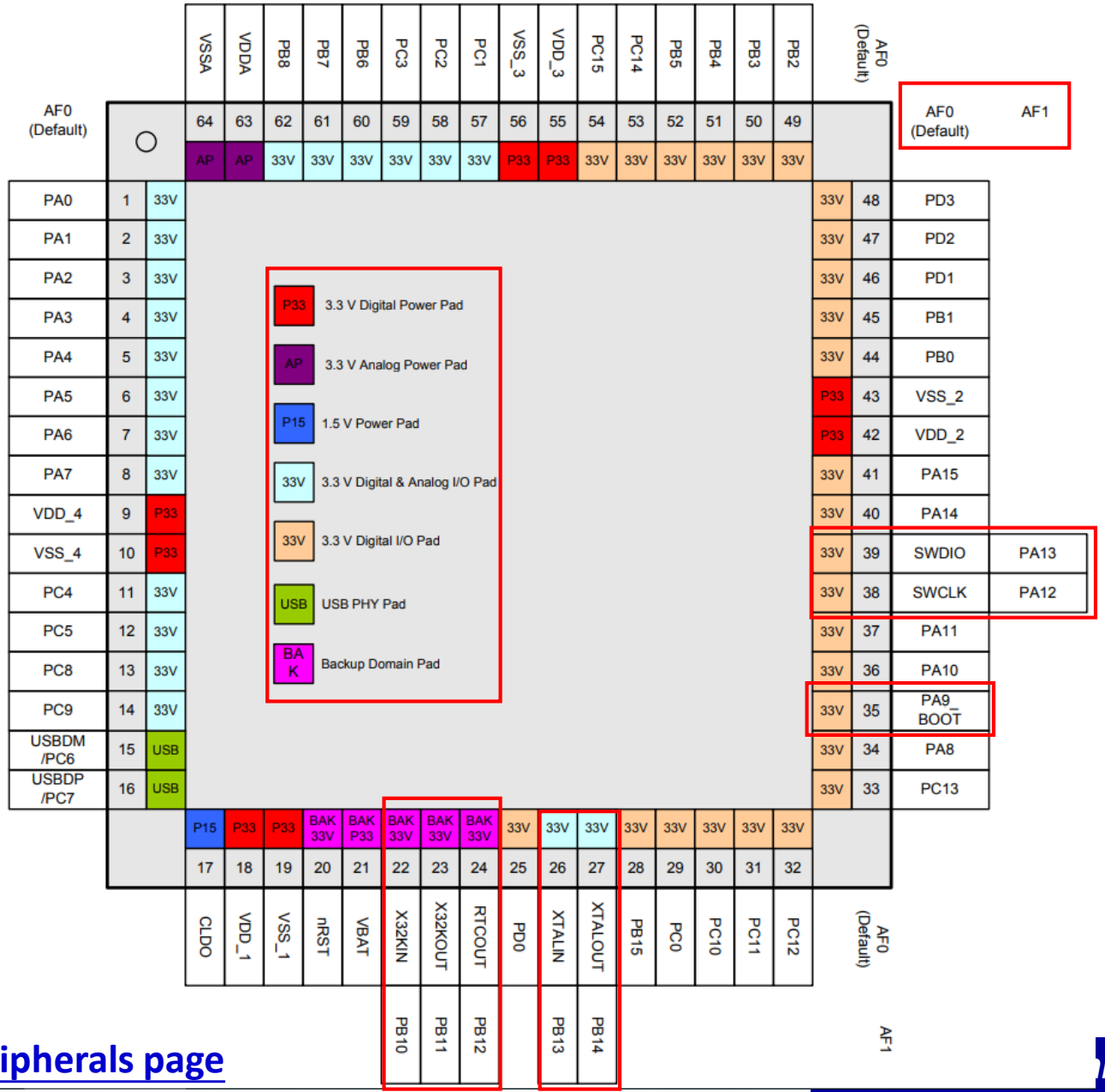
- APB slave interface for register access
- EXTI source selection
- Configurable pin function for each GPIO, up to sixteen alternative functions on each pin
- AFIO lock mechanism



AFIO - Features (2/2)

Package			Alternate Function Mapping														
			AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
64 LQFP	48 LQFP	33 QFN	System Default	GPIO	ADC	CMP	MCTM /GPTM	SPI	USART /UART	I²C	SCI	EBI	I2S	N/A	N/A	SCTM	N/A	System Other
1	1	1	PA0		ADC_ IN0		GT1_ CH0	SPI1_ SCK	USR0_ RTS	I2C1_ SCL	SCI0_ CLK		I2S_WS					
2	2	2	PA1		ADC_ IN1		GT1_ CH1	SPI1_ MOSI	USR0_ CTS	I2C1_ SDA	SCI0_ DIO		I2S_ BCLK					
3	3	3	PA2		ADC_ IN2		GT1_ CH2	SPI1_ MISO	USR0_ TX				I2S_ SDO					
4	4	4	PA3		ADC_ IN3		GT1_ CH3	SPI1_ SEL	USR0_ RX				I2S_SDI					
5	5	5	PA4		ADC_ IN4		GT0_ CH0	SPI0_ SCK	USR1_ TX	I2C0_ SCL	SCI1_ CLK							
6	6	6	PA5		ADC_ IN5		GT0_ CH1	SPI0_ MOSI	USR1_ RX	I2C0_ SDA	SCI1_ DIO							
7	7		PA6		ADC_ IN6		GT0_ CH2	SPI0_ MISO	USR1_ RTS		SCI1_ DET							
8	8		PA7		ADC_ IN7		GT0_ CH3	SPI0_ SEL	USR1_ CTS				I2S_ MCLK					
9			VDD_4															
10			VSS_4															
					ADC		GT0	SPI1	UR0	I2C1		EBI						
							CH2	MISO	TX		CLK	ALE	BCLK					
61	45	29	PB7			CP1	MT_ CH2N			I2C1_ SCL	SCI1_ DET	EBI_ CS1	I2S_ SDO					
62	46	30	PB8			COUT1	MT_ CH3		UR0_ RX	I2C1_ SDA	SCI1_ DIO	EBI_ CS2	I2S_SDI					
63	47	31	VDDA															
64	48	32	VSSA															

AFIO - 64LQFP Pin Assignment



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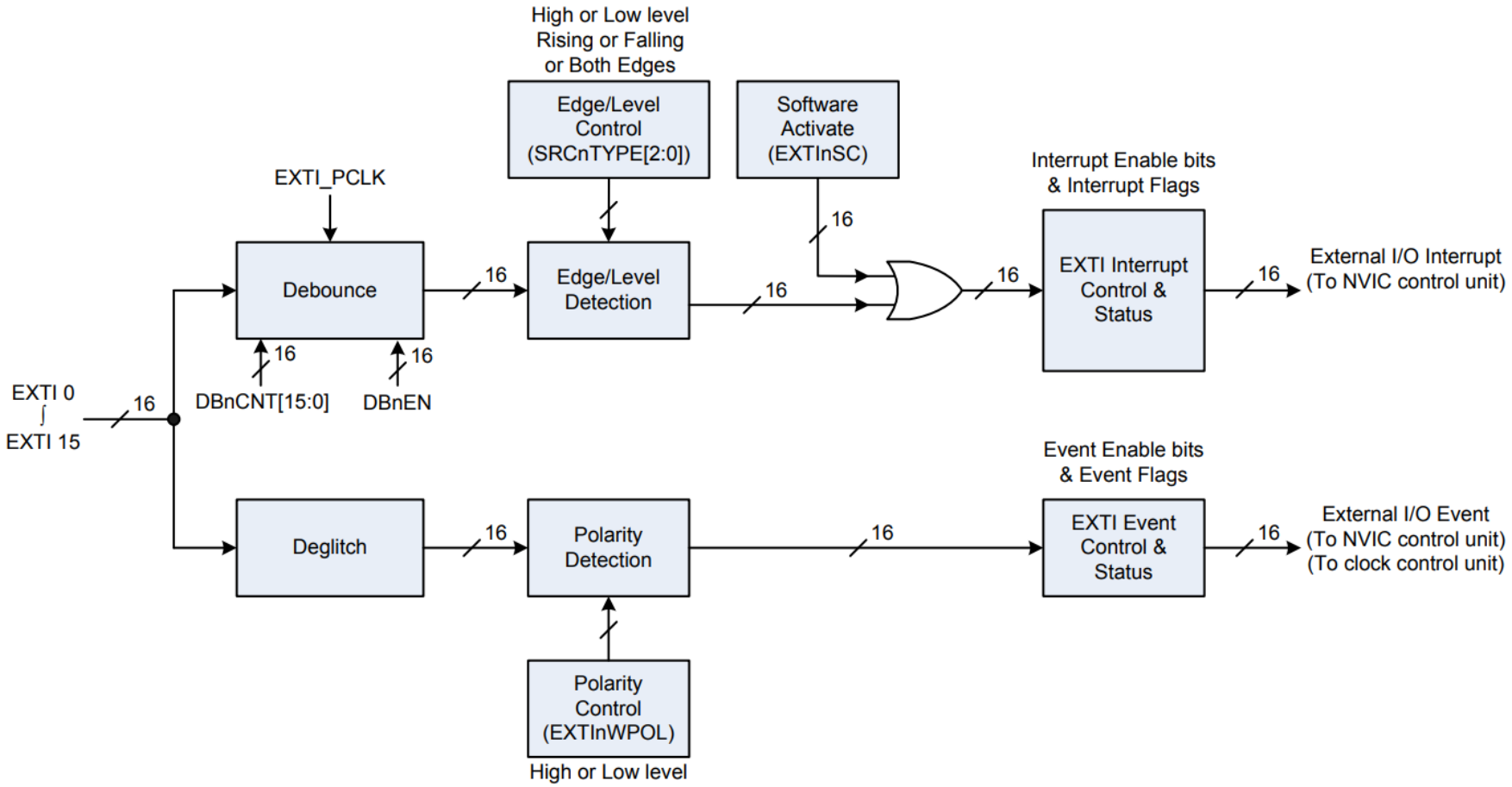
External Interrupt/ Event Controller (EXTI)

EXTI - Block Diagram

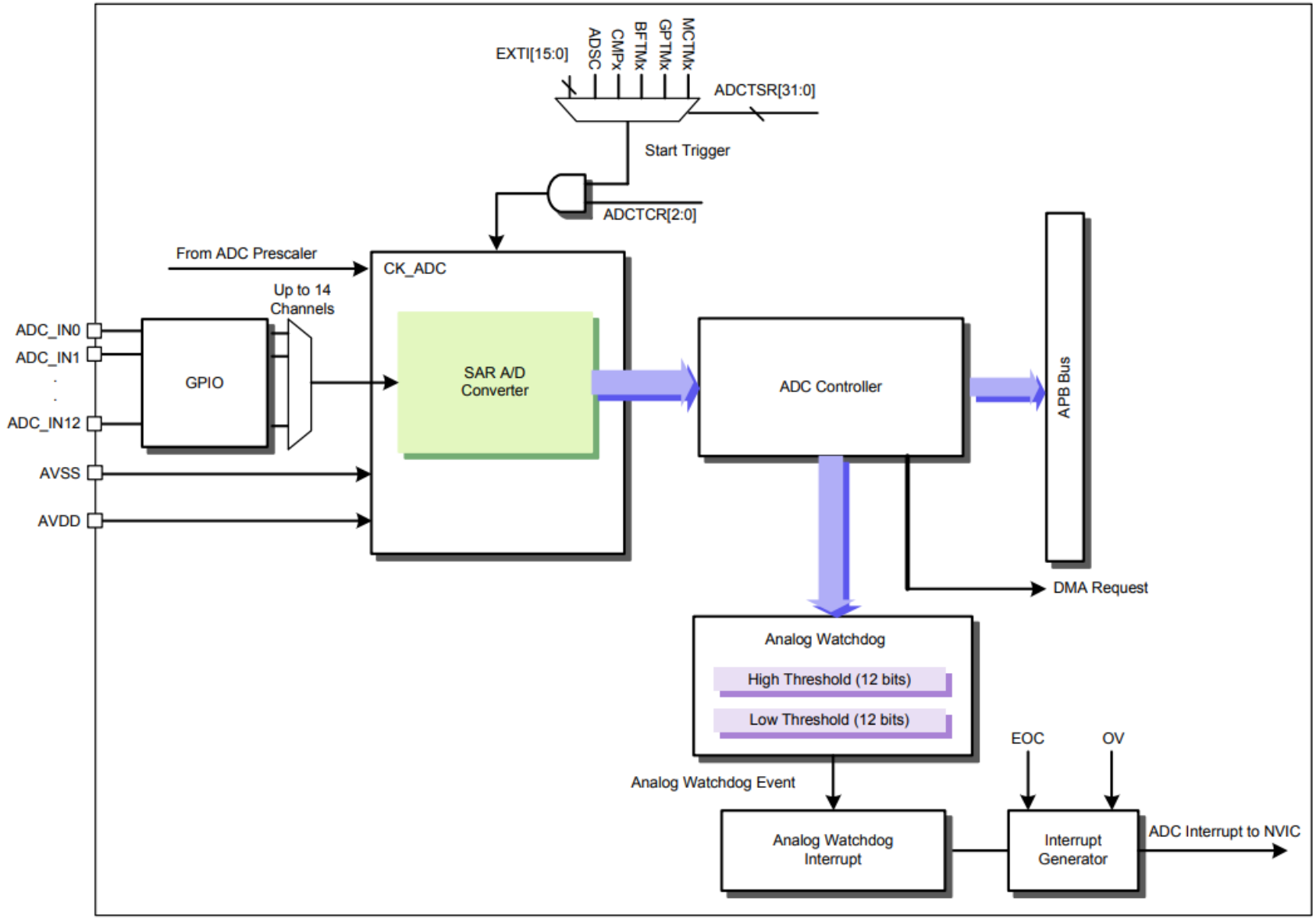


EXTI - Features

- Up to 16 EXTI lines with configurable trigger source and type
  All GPIO pins can be selected as EXTI trigger source
  Source trigger type includes high level, low level, negative edge, positive edge, or both edge
- Individual interrupt enable, wakeup enable and status bits for each EXTI line
- Software interrupt trigger mode for each EXTI line
- Integrated deglitch filter for short pulse blocking

Analog to Digital Converter (ADC)

ADC - Block Diagram



ADC - Features

- 12-bit SAR ADC engine
- Up to 1 MSPS conversion rate
- 12 external analog input channels
- 2 internal analog input channels for reference voltage detection
- Programmable sampling time for conversion channel
- Up to 8 programmable conversion channel sequence and dedicated data registers for conversion result
- Three conversion mode
  - One shot conversion mode
  - Continuous conversion mode
  - Discontinuous conversion mode.
- Analog watchdog for predefined voltage range monitor
  - Lower/upper threshold register
  - Interrupt generation
- Various trigger start source for conversion modes
  - Software trigger
  - EXTI - external interrupt input pin
  - GPTM0 / GPTM1 trigger
  - MCTM trigger
  - BFTM0 / BFTM1 trigger
  - CMP0 / CMP1 trigger
- Multiple generated interrupts
  - End of single conversion
  - End of subgroup conversion
  - End of cycle conversion
  - Analog Watchdog
  - Data register overwriting
- PDMA request on end of conversion occurred

Inter-IC Sound
(I^2S)

I²S - Features

- Master or slave mode
- Mono and stereo
- I²S-justified, Left-justified, and Right-justified mode
- 8/16/24/32-bit sample size with 32-bit channel extended
- 8 × 32-bit TX & RX FIFO with PDMA supported
- 8-bit Fractional Clock Divider with rate control

Cyclic Redundancy Check (CRC)

CRC - Features

- Support CRC16 polynomial: 0x8005, $X^{16}+X^{15}+X^{2}+1$
- Support CCITT CRC16 polynomial: 0x1021, $X^{16}+X^{12}+X^{5}+1$
- Support IEEE-802.3 CRC32 polynomial: 0x04C11DB7, $X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^{8}+X^{7}+X^{5}+X^{4}+X^{2}+X+1$
- Support 1's complement, byte reverse & bit reverse operation on data and checksum
- Support byte, half-word & word data size
- Programmable CRC initial seed value
- CRC computation done in 1 AHB clock cycle for 8-bit data and 4 AHB clock cycles for 32-bit data
- Support PDMA to complete a CRC computation of a block of memory

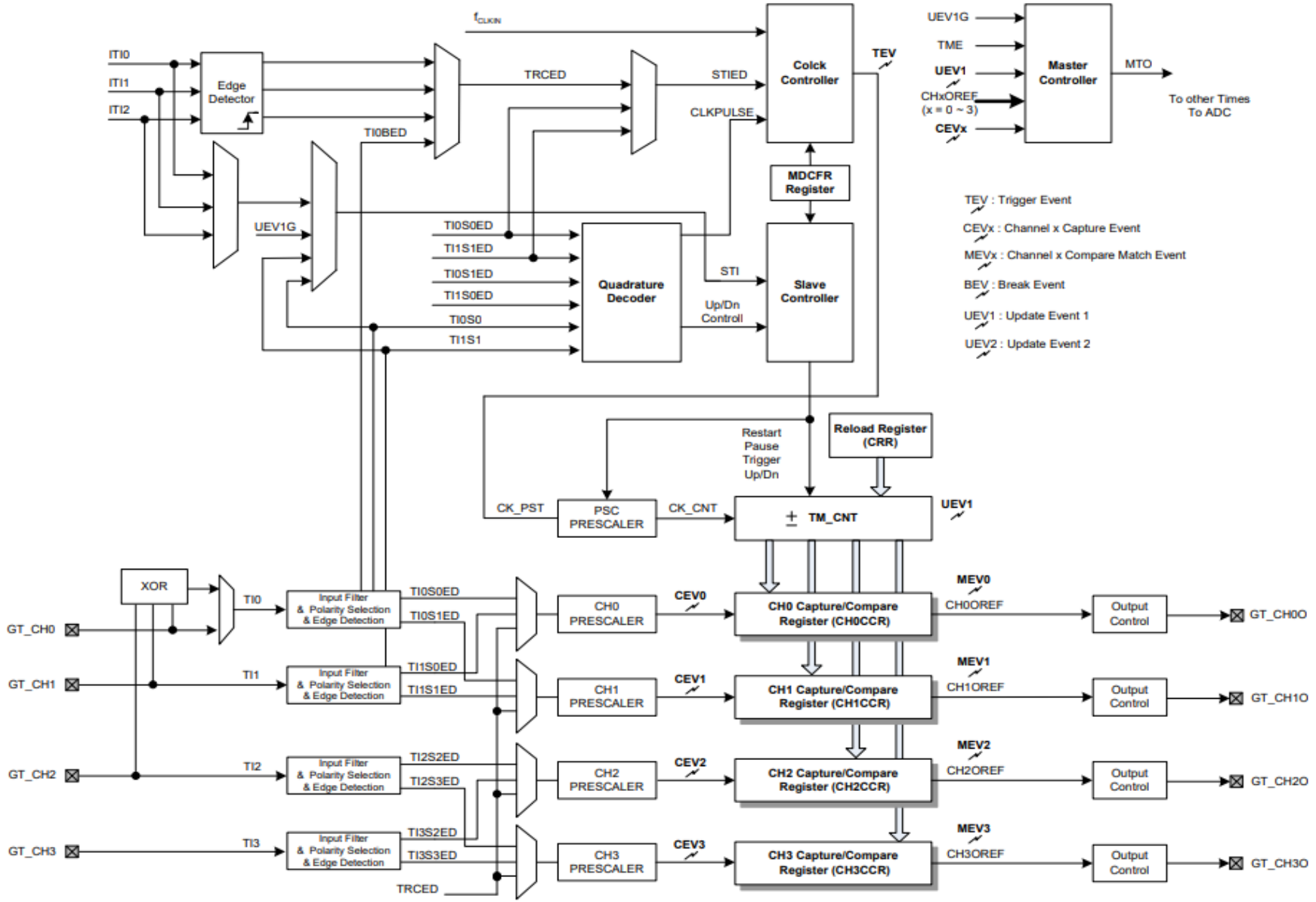
Basic Function Timer (BFTM)

BFTM - Features

- 32-bit up-counting counter
- Compare Match function
- Includes debug mode
- Clock source: BFTM APB clock
- Counter value can be R/W on the fly
- One shot mode: counter stops counting when compare match occurs
- Repetitive mode: counter restarts when compare match occurs
- Compare Match interrupt enable/disable control

General-Purpose Timer (GPTM)

GPTM - Block Diagram

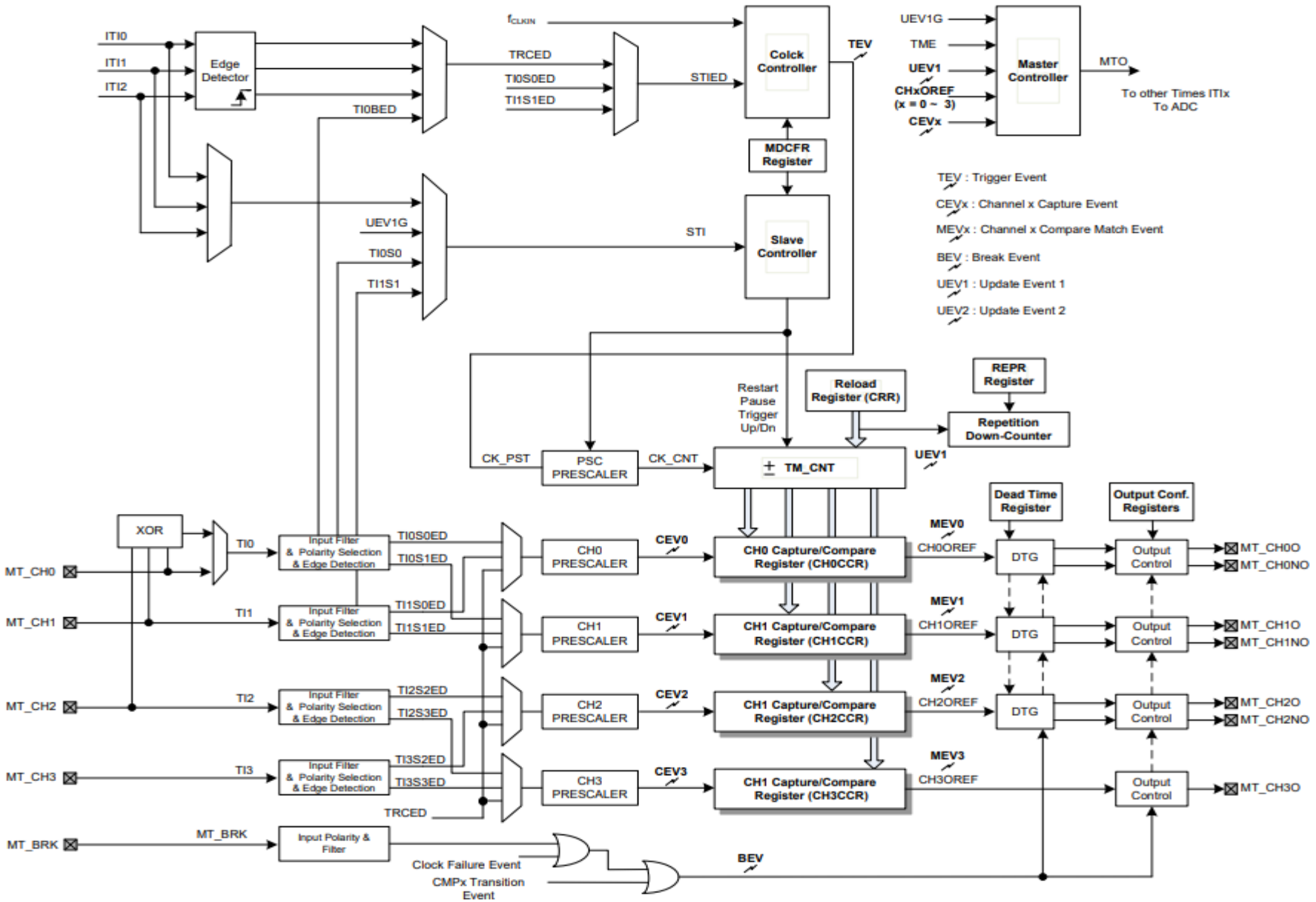


GPTM - Features

- 16-bit up/down auto-reload counter
- 16-bit programmable prescaler that allows division of the counter clock frequency by any factor between 1 and 65536
- Up to 4 independent channels for:
  - Input Capture function
  - Compare Match Output
  - Generation of PWM waveform – Edge and Center-aligned Mode
  - Single Pulse Mode Output
- Encoder interface controller with two inputs using quadrature decoder
- Synchronization circuit to control the timer with external signals and to interconnect several timers together
- Interrupt/PDMA generation with the following events:
  - Update event
  - Trigger event
  - Input capture event
  - Output compare match event
- GPTM Master/Slave mode controller

Motor Control Timer (MCTM)

MCTM - Block Diagram



MCTM - Features

- 16-bit up/down auto-reload counter.
- 16-bit programmable prescaler that allows division the counter clock frequency by any factor between 1 and 65536.
- Up to 4 independent channels for:
  - Input Capture function
  - Compare Match Output
  - PWM waveform Generation – Edge and Center-aligned Counting Mode
  - Single Pulse Mode Output
- Complementary Outputs with programmable dead-time insertion
- Repetition counter updates timer registers only after a given number of counter cycles.
- Synchronization circuit controls the timer with external signals and can interconnect several timers together.
- Interrupt/PDMA generation on the following events:
  - Update event 1
  - Update event 2
  - Trigger event
  - Input capture event
  - Output compare match
  - Break event – only interrupt
- MCTM Master/Slave mode controller
- Supports 3-phase motor control and hall sensor interface
- Break input signals to assert the timer output signals in reset state or in a known state

Real Time Clock (RTC)

RTC - Features

- 32-bit up counter for counting elapsed time
- Programmable clock prescaler
  - Division factor: 1, 2, 4, 8, …, 32768
- 32-bit compare register for alarm usage
- RTC clock source
  - LSE oscillator clock
  - LSI oscillator clock
- Three RTC Interrupt/wakeup settings
  - RTC second clock interrupt/wakeup
  - RTC compare match interrupt/wakeup
  - RTC counter overflow interrupt/wakeup
- The RTC interrupt/wakeup event can work together with power management to wake up the chip from power saving mode

Watchdog Timer (WDT)

WDT - Features

- Clock source from either internal 32 kHz RC oscillator (LSI) or 32,768 Hz oscillator (LSE)
- Can be independently setup to keep running or to stop when entering the sleep or deep sleep mode 1
- 12-bit down counter with 3-bit prescaler structure
- Provides reset to the system
- Limited reload window setup function for custom Watchdog timer reload times
- Watchdog Timer may be stopped when the processor is in the debug
- Reload lock key to prevent unexpected operation
- Configuration register write protection function for counter value, reset enable, delta value, and prescaler

Communication Peripherals

Communication (1/3)

- Inter-integrated Circuit (I^2C) x 2
  - Master and Slave mode
  - 100 KHz, 400 KHz, 1 MHz
  - 7-bit and 10-bit addressing mode
- Serial Peripheral Interface (SPI) x 2
  - Master and Slave mode
  - Slave : 16 MHz
  - Master : 24 MHz
  - FIFO : 8 levels
- Universal Synchronous Asynchronous Receiver Transmitter (USART) x 2
  - RS232 / RS485 / IrDA / SPI Master
  - Hardware flow control
  - 4.5 MHz
  - FIFO: 16 levels

Communication (2/3)

- Universal Asynchronous Receiver Transmitter (UART) x 2
  - RS232
  - 3 MHz
  - FIFO: 16 levels

- Universal Serial Bus Device Controller (USB)
  - USB 2.0 Full Speed (12 Mbps)
  - 1 control endpoint (EP0)
  - 3 single-buffered endpoint (EP1~EP3)
    - Bulk / Interrupt transfer
  - 4 double-buffered endpoint (EP4~EP7)
    - Bulk / Interrupt / Isochronous transfer
  - 1024 bytes EP-SRAM

Communication (3/3)

- Smart Card Interface (SCI)
  - Supports ISO 7816-3 standard
- Extend Bus Interface (EBI)
  - Asynchronous static random access memory – SRAM
  - Read-only memory – ROM
  - NOR Flash
  - 8-/16-bit parallel bus CPU interface

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Thanks